REMARKS

The Examiner is thanked for the thorough examination of the present application and the indication that claims 38 and 39 contain allowable subject matter. Responsive to the Office Action, Applicant has made the foregoing amendments to place the application in condition for allowance. No new matter has been added by this amendment. In this paper, claims 1 and 18-35 are amended, and claim 52 is added. Support for the amendment can be found, for example, FIG. 7a and FIG. 8a of the present invention.

The Office Action objected to the Abstract because the first line of the abstract characterized the inventive flash memory cesss as "improved." Applicant has amended the Abstract herein to address this objection, and requests that the objection with withdrawn.

The Office Action objected to claims 19-34 because of certain informalities (i.e., line 1 of each claim referring to the "structure" rather than the "method" of claim 18). Applicant has amended each of these claims to correct this informality, and these objections should be withdrawn.

Objections Under 35 U.S.C. 112

Claims 1-3, 6-20, 23-37 and 40-48 were rejected under 35 U.S.C 112 as allegedly indefinite for failing to particularly the subject matter that Applicant regards as the invention. Specifically, the Office Action stated that claims 1, 18, and 35 draw reference to "type one" and "type two" isolation regions, but alleges that this reference is vague. Applicant has amended claims 1, 18, and 35 to address and overcome these rejections.

Rejections Under 35 U.S.C. 102(a)

Claim 1-14 and 18-27 were rejected under 35 U.S.C. 102(a) as allegedly anticipated by admitted prior art APA. Applicant asserts that independent claims 1 and 18 (as amended) are patentable for at least the reasons discussed below.

Independent claim 1, as amended, recites:

> 1. A structure for flash memory cells, comprising:
> a semiconductor region within a substrate;
> first isolation regions, separating cells, and second isolation regions, separating programming bit line channel regions of a cell from reading bit line channel regions of a cell, delineating active regions contained within said semiconductor region;
> a conductive floating gate, for each cell, having a first floating gate portion disposed over the active region in the programming bit line channel region of a cell and a second floating gate portion disposed over the active region in the reading bit line channel region of the cell, both said first and said second floating gate portions being separated from said active regions by a floating gate insulator layer disposed over said active regions, and a third floating gate portion passing over said second isolation region to connect said first floating gate portion and second floating gate portion, ***wherein width of said first floating gate portion is narrower than width of said second floating gate portion***;
> a conductive control gate separated from said floating gate by an intergate insulator layer and from said semiconductor region by a control gate insulator layer and having a first control gate portion entirely disposed over said first floating gate portion, where said first floating gate portion completely covers the space between a first source region and a first drain region, having a second control gate portion disposed over said second floating gate portion, where said second floating gate portion does not extend all the way from a second source region to second drain region, said second control gate region completing the covering of the space between said second source region and said second drain region and having a third control gate portion disposed over said third floating gate portion and connecting said first control gate portion and second control gate portion;
> a covering insulator layer with a programming bit line channel contact line disposed over said covering insulator layer and connecting to said first drain region through said covering insulator layer and a reading bit line channel contact line disposed over said covering insulator layer and connecting to said second drain region through said covering insulator layer.

(Emphasis Added)

As expressly recited, the structure of the flash memory cells of amended claim 1 comprise a width of said first floating gate portion being narrower than width of said second floating gate portion.

Referring to FIG. 2a, it is clear that APA teaches all portions of the floating gate 8 having the same width. Significantly, APA does not disclose or suggest "***width of said first floating gate portion is narrower than width of said second floating gate portion,***" as expressly recited in amended claim 1.

The MPEP requires that a reference teach EVERY element of a claim in order to anticipate the claim. Specifically, MPEP Section 2131 states:

> "***A claim is anticipated only if each and every element as set forth in the claim is found***, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). >"When a claim covers several structures or compositions, either generically or as alternatives, the claim is deemed anticipated if any of the structures or compositions within the scope of the claim is known in the prior art." Brown v. 3M, 265 F.3d 1349, 1351, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) (claim to a system for setting a computer clock to an offset time to address the Year 2000 (Y2K) problem, applicable to records with year date data in "at least one of two-digit, three-digit, or four-digit" representations, was held anticipated by a system that offsets year dates in only two-digit formats). See also MPEP § 2131.02.< "***The identical invention must be shown in as complete detail as is contained in the ... claim.***" Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Note that, in some circumstances, it is permissible to use multiple references in a 35 U.S.C. 102 rejection. See MPEP § 2131.01.

It is clear that not every element as set forth in the amended claim 1 is found in APA. Consequently, Applicant respectfully requests reconsideration and withdrawal of this rejection.

Likewise, independent claim 18, as amended, recites:

> 18. A method of forming flash memory cells, comprising:
> providing a semiconductor region within a substrate;
> forming first isolation regions, separating cells, and forming second isolation regions, separating programming bit line channel regions of a cell from reading bit line channel regions of a cell, first isolation regions and second isolation regions delineating active regions contained within said semiconductor region;
> forming a conductive floating gate, in each cell, where a first floating gate portion is disposed over the active region in the programming bit line channel region of a cell and a second floating gate portion is disposed over the active region in the reading bit line channel region of the cell, both said first and said second floating gate portions being separated from said active regions by a floating gate insulator layer formed over said active regions, and a third floating gate portion passes over said second isolation region to

connect said first floating gate portion and second floating gate portion, ***wherein width of said first floating gate portion is narrower than width of said second floating gate portion;***

forming a conductive control gate separated from said floating gate by an intergate insulator layer formed over said floating gate and from said semiconductor region by a control gate insulator layer formed over the active region and where a first control gate portion is entirely disposed over said first floating gate portion, where said first floating gate portion is formed to completely cover the space between a first source region and a first drain region, and a second control gate portion is disposed over said second floating gate portion, where said second floating gate portion is formed so as not to extend all the way from a second source region to second drain region, said second control gate region being formed to complete the covering of the space between said second source region and said second drain region and with a third control gate portion formed to be disposed over said third floating gate portion and connecting said first control gate portion and second control gate portion;

forming a covering insulator layer and forming a programming bit line channel contact line disposed over said covering insulator layer and connecting to said first drain region through said covering insulator layer and forming a reading bit line channel contact line disposed over said covering insulator layer and connecting to said second drain region through said covering insulator layer.

(Emphasis Added)

Like claim 1, claim 18 expressly recites that the width of said first floating gate portion is narrower than width of said second floating gate portion.

Referring to FIG. 3a and 3b, it is clear that APA teaches all portions of the control gate 12 having the same width. APA, however, does not disclose or suggest "***width of said first floating gate portion is narrower than width of said second floating gate portion***" in amended claim 18.

Therefore, not every element as set forth in the amended claim 18 is found in APA. Consequently, Applicant respectfully submits that APA fails to disclose the feature above-discussed in the present invention as set forth in amended claim 18. Reconsideration of this rejection is hereby respectfully requested.

Claim 1 and 18 are independent claims, on which claims 2-14 and 19-27 respectively depend. Applicant asserts that amended claim 1 and 18 are patentable for the reasons discussed, and therefore for at least the same reasons, claims 2-14 and 19-27 are patentable.

Rejections Under 35 U.S.C. 103(a)

Claims 15-17 and 28-34 were rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art APA.

Claim 1 and 18 are independent claims, on which claims 15-17 and 28-34 respectively depend. Applicant asserts that amended claim 1 and 11 are patentable for the reasons discussed, and therefore for at least the same reasons, claims 15-17 and 28-34 are patentable.

Newly added claim

New claim 52 has been added, and it is respectfully that these rejections be withdrawn.

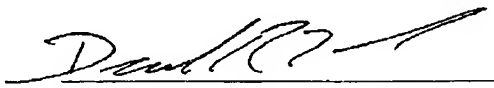
The applicant has reviewed the prior art as cited by the Examiner but not used in the rejection and believe that the amended claims and the new claims clearly and distinctly patentably define over such prior art.

CONCLUSION

Applicants respectfully request submit that the foregoing is fully responsive to the election request and that all presently-pending claims be allowed to issue. If the Examiner has any questions or comments regarding Applicants' response, the Examiner is encouraged to telephone the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,



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Annotated Sheet

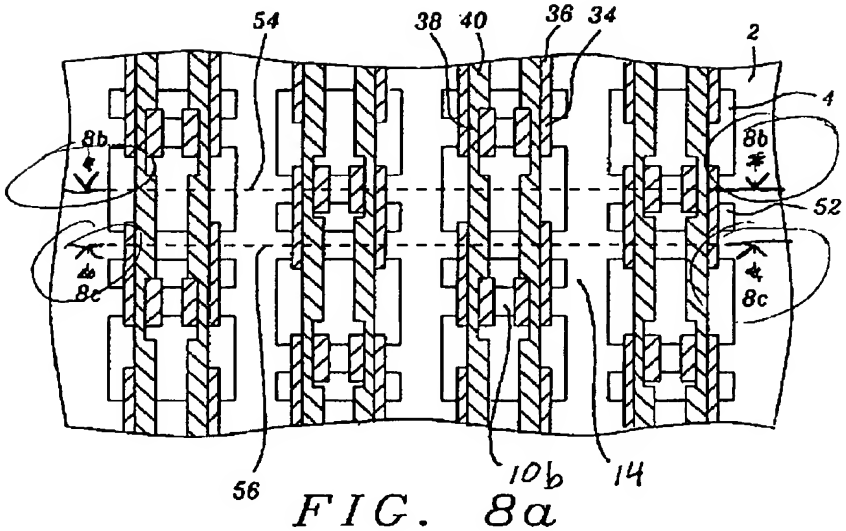

FIG. 8a

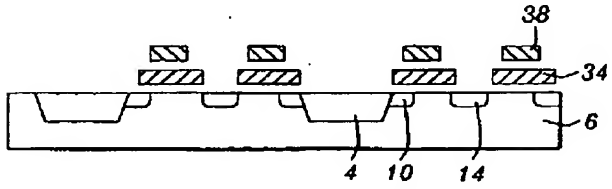

FIG. 8b

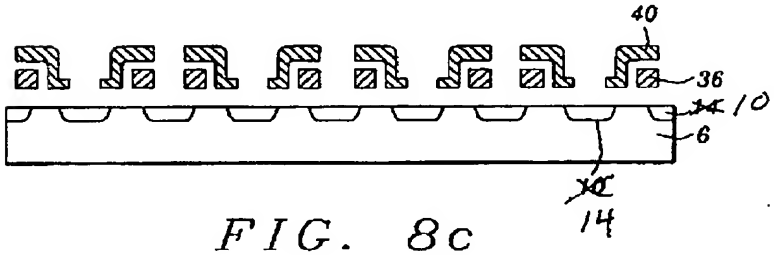

FIG. 8c

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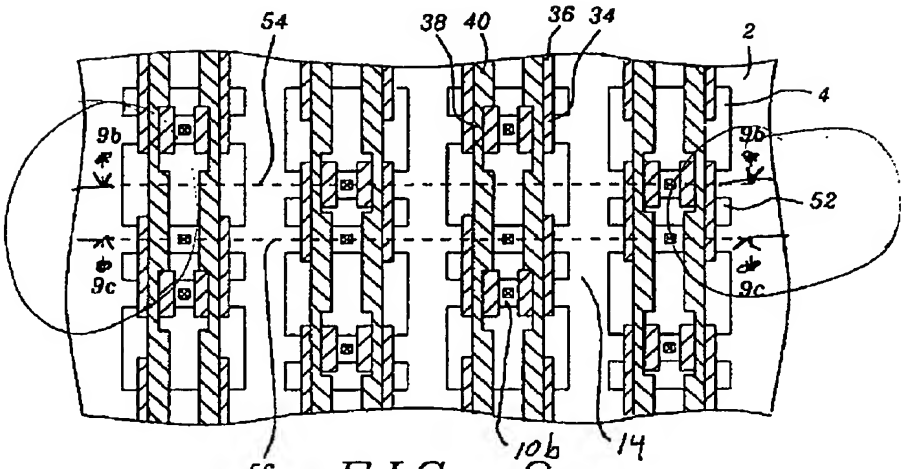

FIG. 9a

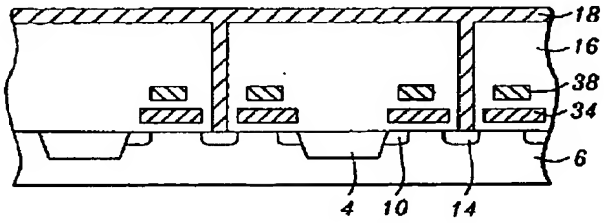

FIG. 9b

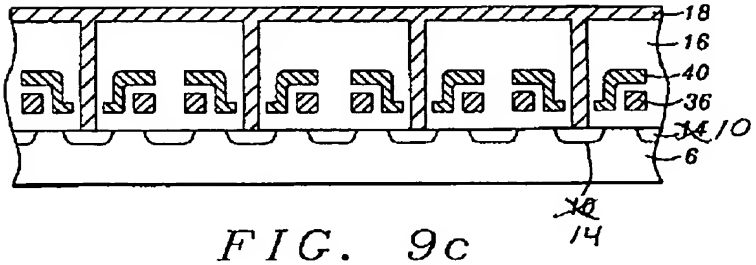

FIG. 9c

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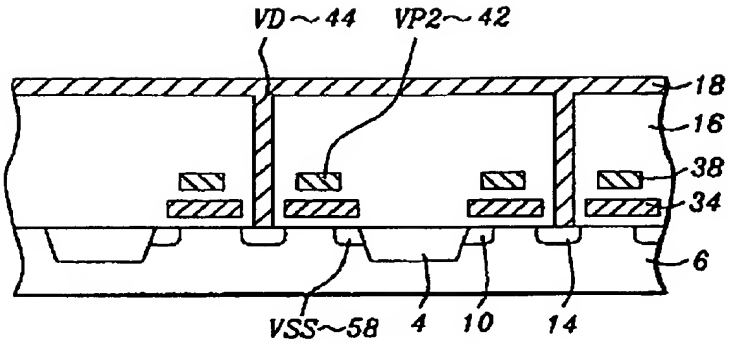

FIG. 10a

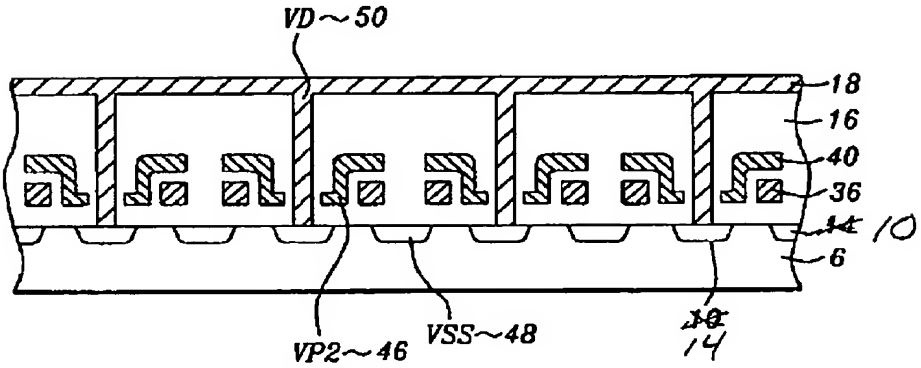

FIG. 10b